

66/06/10
07/30/99
JCS30 U.S. PTO
09/365211

Case Docket No. PHO 98,532

A

THE COMMISSIONER OF PATENTS AND TRADEMARKS, Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor(s):

KLAUS ULLY

For: DATA PROCESSING DEVICE WITH DATA PROCESSING MEANS UTILIZING A
CHARACTERISTIC VALUE AND WITH MEANS FOR COUNTERACTING ANALYSIS
METHODS FOR THE DETECTION OF THE CHARACTERISTIC VALUE

ENCLOSED ARE:

- ☒ Associate Power of Attorney;
☐ Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;
☒ Preliminary Amendment;
☒ Specification (16 Pages of Specification, Claims, & Abstract);
☒ Declaration and Power of Attorney:
(1 Pages of a ☐ fully executed ☒ unsigned Declaration);
☒ Drawing (2 sheets of ☐ informal ☒ formal sheets);
☒ Certified copy of Europe application Serial No. 98890222.7;
☒ Other: Related Cases/Technology Report
☐ Assignment to

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - 760.00
Total Claims	14 - 20 =	0	X \$18 =	0.00
Independent Claims	2 - 3 =	0	X \$78 =	0.00
Multiple Dependent Claims, if any			\$260 =	0.00
TOTAL FILING FEE			=	\$760.00

Please charge Deposit Account No. 14-1270 in the amount of the total filing fee indicated above, plus any deficiencies. The Commissioner is also hereby authorized to charge any other fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

☐ Amend the specification by inserting before the first line the sentence: --This is a continuation-in-part of application Serial No. , filed .--.

CERTIFICATE OF EXPRESS MAILING

Express Mail Mailing Label No. EL215005424

Date of Deposit July 30, 1999
I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Noemi Chapa
Printed Name

Noemi Chapa
Signature

Gregory L. Thome
Gregory L. Thome, Reg. No. 39,398
Attorney
(914) 333-9665
U.S. Philips Corporation
580 White Plains Road
Tarrytown, New York 10591
F:\WPDOCS\TH\MK27THA0.NC0.doc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

KLAUS ULLY

PHO 98,532

Serial No.

Filed: CONCURRENTLY

Title: DATA PROCESSING DEVICE WITH DATA PROCESSING MEANS UTILIZING A
CHARACTERISTIC VALUE AND WITH MEANS FOR COUNTERACTING ANALYSIS
METHODS FOR THE DETECTION OF THE CHARACTERISTIC VALUE

Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please
amend the above-identified application as follows:

IN THE SPECIFICATION

Page 1,	above line 1,	insert the heading: --BACKGROUND OF THE INVENTION--;
Page 3,	above line 12,	insert the heading: --SUMMARY OF THE INVENTION--;
Page 4,	above line 25,	insert the heading: --BRIEF DESCRIPTION OF THE DRAWINGS--;
Page 5,	above line 1,	insert the heading: --DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS--;

IN THE ABSTRACT


Page 16, last line, delete "(Fig. 1.)".

REMARKS

The specification has been amended add headings in accordance with MPEP Section 601.

The above amendments are submitted to place this application in proper U.S. format. Entry of the amendment and an early action on the merits are solicited.

Respectfully submitted,

By 
Gregory L. Thorne, Reg. No. 39,398
Attorney
(914) 333-9665

Data processing device with data processing means utilizing a characteristic value and with means for counteracting analysis methods for the detection of the characteristic value

The invention relates to a data processing device which includes a circuit which consists of various circuit sections which can be fed with a supply voltage via a configuration of conductors, and includes data processing means which constitute such a circuit section that can be fed with the supply voltage and are arranged to process data while utilizing a
5 characteristic value, and also includes sequencing means which also constitute such a circuit section that can be fed with the supply voltage and are arranged to execute an algorithm in order to control the data processing means in conformity with this algorithm, which algorithm comprises a given number N of sub-algorithms which contain identical sequences of algorithm steps and can be executed in a given order each time when the algorithm is executed, and
10 wherein, upon processing of data by means of the data processing means under the control of the sequencing means in conformity with the algorithm, the data processing causes a current peak pattern to occur at the area of the configuration of conductors, the pattern configuration of the current peak pattern being dependent on the algorithm steps, on the processed data and on the characteristic value.

15 The invention also relates to a circuit for a data processing device which consists of various circuit sections which can be fed with a supply voltage via a configuration of conductors and includes data processing means which constitute such a circuit section that can be fed with the supply voltage and are arranged to process data while utilizing a characteristic value, and also includes sequencing means which also constitute such a circuit
20 section that can be fed with the supply voltage and are arranged to execute an algorithm in order to control the data processing means in conformity with this algorithm, which algorithm comprises a given number N of sub-algorithms which contain identical sequences of algorithm steps and can be executed in a given order each time when the algorithm is executed, and wherein, upon processing of data by means of the data processing means under the control of
25 the sequencing means in conformity with the algorithm, the data processing causes a current peak pattern to occur at the area of the configuration of conductors, the pattern configuration

of the current peak pattern being dependent on the algorithm steps, on the processed data and on the characteristic value.

5 A data processing device of the kind set forth in the first paragraph and a circuit of the kind set forth in the second paragraph are known notably from the contact-type chip cards which are used in a variety of versions and include an integrated component developed and marketed by Applicant. In the known data processing device, so in the known contact-type chip card, and in the known circuit, so in the integrated component included in such a known
10 contact-type chip card, the data processing means are formed by encryption means which perform, in conformity with the "Data Encryption Standard" (DES), an encryption operation on data applied thereto while utilizing a characteristic value which is also applied thereto, that is to say a secret key. During such an encryption operation overall $N = 8$ so-called SBOX units are executed, an SBOX result being calculated by means of each SBOX unit. All eight SBOX
15 units are executed within the framework of a program which constitutes an algorithm and each program block of which forms a sub-algorithm and corresponds to an SBOX unit. Each program block, corresponding to an SBOX unit, contains a table which is characteristic of the relevant SBOX unit and contains entries, the entries of all SBOX units being different. The table contained in an SBOX unit, or the entries in this table, is used to determine output data
20 associated with the input data applied to an SBOX unit. Such determination of output data associated with input data, however, is performed while utilizing the same algorithm for the linking of input data and output data in all eight SBOX units; this means that each of the N program blocks, representing a respective SBOX unit and constituting a respective sub-algorithm, contains identical sequences of program instructions as algorithm steps. In the
25 known data processing device, or the known circuit, the N program blocks are invariably executed in the same order each time when the program is executed.

During execution of an encryption operation a current peak pattern occurs at the area of the configuration of conductors, which peak pattern is dependent on the program instructions, on the data processed in the encryption means and on the characteristic value
30 used in the encryption means, so on the secret key for these encryption means. In the known data processing device, or in the known circuit, a problem is encountered in that the respective current peak patterns thus caused also occur in parts of the circuit, or parts of the data processing device, which can be externally interrogated. The occurrence of the respective current peak patterns each time caused in said parts can be used, for example, to supply the

data processing means for the processing of data while utilizing a characteristic value with given known data an arbitrary number of times in succession in order to carry out processing, and to subject the current peak pattern thus produced, always being the same, during the processing of this known data, to observation or detection, so that information concerning the characteristic value, so the secret key, used in the data processing means, so the encryption means, can be extracted from the detected current peak pattern while using rather complex correlation methods or comparison methods which, however, are known and available. Evidently, such cracking of a secret key is undesirable, because the desired secrecy can then no longer be reliably ensured.

It is an object of the invention to avoid the described problems and to provide, while using simple means and only very little additional work, an improved data processing device, or an improved circuit for a data processing device, which ensures a high degree of reliability in respect of keeping a characteristic value secret.

In order to achieve the described object, a data processing device of the kind set forth in the first paragraph according to the invention is characterized in that the circuit additionally includes order fixation means which co-operate with the sequencing means and whereby, upon each execution of the algorithm, an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms.

In order to achieve the described object, furthermore, a circuit of the kind set forth in the second paragraph according to the invention is characterized in that the circuit additionally includes order fixation means which cooperate with the sequencing means and whereby, for each execution of the algorithm, an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms.

By taking the steps according to the invention, it is very simply and reliably achieved that even though the succession of all algorithm steps of all successively executed sub-algorithms is always the same for each execution of the algorithm, the order for the execution of the N sub-algorithms of an algorithm is different for each execution of the algorithm, so that the order of the execution of the N sub-algorithms cannot be determined from outside the data processing device or the circuit of the data processing device. Therefore, it is also impossible to compare successively produced current peak patterns, caused by successive activation of the algorithm, in order to use these peak patterns for analysis by means of correlation methods or comparison methods. Undesirable recognition or detection of

a characteristic value used in the data processing means, such as a secret key, thus becomes practically impossible or at least drastically more difficult.

The steps disclosed in the Claims 2 and 3 or 7 and 8 have proven to be very effective for data processing according to the invention, or for a circuit according to the invention, because these embodiments are characterized by a pronounced simplicity and can be readily implemented while using means already present in a data processing device according to the invention or a circuit according to the invention. As regards the order selection means it is to be noted that these order selection means preferably contain only a part of all feasible orders for the execution of the N algorithms, but that it is also simply possible to provide the order selection means with all feasible orders for the execution of N sub-algorithms.

It has been found that the steps according to the invention are particularly advantageously taken in a data processing device in conformity with Claim 4 or a circuit as claimed in Claim 9, because there is a very pronounced need for secrecy as regards the key used notably in the case of means for the encryption and/or decryption of data.

A data processing device according to the invention may be formed, for example by a computer or a personal computer arranged, for example to execute an encryption program. The steps according to the invention have proved to be very attractive notably for a data processing device as disclosed in Claim 7 or in a circuit as disclosed in Claim 14, because the risk of cracking of a characteristic value is particularly high in these cases.

These and other aspects of the invention will become apparent from the embodiment described hereinafter.

The invention will be described in detail hereinafter with reference to an embodiment as shown in the drawings, however, without the invention being restricted thereto.

Fig. 1 shows a block diagram of an in this context essential part of a data processing device and a circuit for this data processing device in a first embodiment of the invention.

Fig. 2 shows diagrammatically three executions of one and the same program which consists of a total of N program blocks.

Fig. 1 shows a block diagram of a part of a data processing device which is in this case formed by a data carrier 1 which is constructed for contactless communication with a write/read station which is provided for this purpose but not shown in Fig. 1.

The data carrier 1 includes a circuit 2 which is realized in integrated technology. The circuit 2 consists of a plurality of circuit sections which will be described in detail hereinafter. The circuit sections can be supplied with a supply voltage V via a configuration of conductors 3, said supply voltage being a DC supply voltage. The generating of the supply voltage V will also be described in detail hereinafter.

The data carrier 1 includes transmitter/receiver means 4 which include a transmitter coil 5. The receiver/transmitter means 4 are connected to a first connection 6 and to a second connection 7 of the circuit 2. The transmitter coil 5 can be inductively coupled to a transmitter coil of a write/read station not shown. These two transmitter coils enable a non-modulated carrier signal CS as well as an amplitude modulated carrier signal CSM, being amplitude modulated in conformity with data DA to be transmitted from the write/read station to the data carrier 1, as well as a load modulated carrier signal CSB, which can be generated by means of load modulation means (not shown in Fig. 1) of the data carrier 1, or the circuit 2 of this data carrier 1, and whereby data to be transmitted from the data carrier 1 to a write/read station can be transmitted, to be transmitted between the two communicating partners, so a write/read station and the data carrier 1. The foregoing are facilities which have since long been known.

The supply voltage V can be obtained in the data carrier 1 by means of the non-modulated carrier signal CS transmitted from a write/read station to the data carrier 1 and by means of the amplitude modulated carrier signal CSM transmitted from a write/read station to the data carrier 1. To this end, the non-modulated carrier signal CS received by the receiver/transmitter means 4 and the amplitude modulated carrier signal CSM are applied, via the first connection 6 and an electrically conductive connection 8 connected to the first connection 6, to supply voltage generating means 9. The supply voltage generating means 9 essentially consist of a rectifier stage and a storage capacitor as well as voltage-limiting means which prevent an undesirable overvoltage. The supply voltage generating means 9 are capable of generating the already mentioned supply voltage V which can be output to the configuration of conductors 3 via an output 10 of the supply voltage generating means 9. The generated supply voltage V can be applied to the various circuit sections of the circuit 2 via the configuration of conductors 3. It is to be noted that this configuration of conductors 3 also

includes conductive ground connections which, however, have been omitted in Fig. 1 for the sake of simplicity.

The data carrier 1, or the circuit 2, includes first data processing means 11 which can be supplied with the supply voltage V via a supply input 12. Furthermore, via a connection 13A the first data processing means 11 can also be supplied with the amplitude modulated carrier signal CSM output by the receiver/transmitter means 4. The load modulated carrier signal CSB can be obtained in the receiver/transmitter means 4 by way of the first data processing means 11, via a further connection 13B which is connected to the second connection 7. Furthermore, a first BUS connection 14, connected to sequencing means 15, is connected to the first data processing means 11. The sequencing means 15 are arranged to execute a first algorithm in order to control the first data processing means 11 in conformity with this first algorithm.

The first data processing means 11 include demodulation means (not shown) whereby the applied amplitude modulated carrier signal CSM can be demodulated. After such demodulation of the amplitude modulated carrier signal CSM, if necessary, the demodulated signal can be decoded. If desired, further processing operations may also be performed. After the execution of all processing operations, the first data processing means 11 output data DA via a second BUS connection 16 which is connected to second data processing means 17.

The second data processing means 17 are arranged to process data DA while using a characteristic value CV. In the present case the second data processing means 17 are formed by means for the encryption and/or decryption of data, the secret key required for the encryption and decryption being formed by the previously mentioned characteristic value CV.

The second data processing means 17 include a supply input 18 via which the second data processing means 17 can be supplied with the supply voltage V. Furthermore, a third BUS connection 19 is connected to the second data processing means 17, the other end of said bus connection being connected to the sequencing means 15. The sequencing means 15 are also arranged to execute a second algorithm in order to control the second data processing means 17 in conformity with this second algorithm.

In the present embodiment of the data carrier 1 of Fig. 1 the circuit 2 includes program storage means 20 which co-operate with the sequencing means 15 and in which the second algorithm is stored in the form of a program P. The second algorithm, so the program P, contains a given number N of sub-algorithms which are in this case formed by N program blocks PB1, PB2, PB3 ... PBN. The sub-algorithms, formed by the program blocks PB1 to PBN, contain identical successions of algorithm steps which are formed by program

instructions CO1, CO2, CO3 ... COR in the present case. The N sub-algorithms, so the N program blocks, can be executed in a given order during each execution of the algorithm, so of the program P, as will be described in detail hereinafter. The program storage means 20 are connected, via a fourth BUS connection 21, to the sequencing means 15 so that co-operation
5 between the program storage means 20 and the sequencing means 15 is possible via the fourth BUS connection 21. The program storage means 20 include a supply input 22 via which the supply voltage V can be applied to the program storage means 20.

The circuit 2 also includes storage means 23 which comprise a data storage section 24 and a characteristic value storage section 25. The data storage section 24 is
10 arranged to store data DA. The characteristic value storage section 25 is arranged to store a characteristic value CV. The storage means 23 include a supply input 26 via which the supply voltage V can be applied to the storage means 23. A fifth BUS connection 27 is connected to the storage means 23, the other end of said BUS connection being connected to the second data processing means 17. Bi-directional transport of data between the second data processing
15 means 17 and the storage means 23 and transport of the characteristic value CV from the storage means 23 to the second data processing means 17 can take place via the fifth BUS connection 27. As is denoted by dashed lines in Fig. 1, a separate BUS connection 28 may be provided between the characteristic value storage section 25 and the second data processing means 17, said separate BUS connection enabling an exchange of at least a characteristic value
20 CV between the characteristic value storage section 25 and the second data processing means 17.

Data DA applied from the first data processing means 11 to the second data processing means 17, via the second BUS connection 16, can be encrypted in the course of an encryption operation in the second data processing means 17. In the case of such an encryption
25 operation, the encrypted data DA produced is applied, via the fifth BUS connection 27, to the data storage section 24 of the storage means 23 so as to be stored therein.

Data DA which is applied to the second data processing means 17, via the bus connection 27, and read from the data storage section 24 of the storage means 23 can be encrypted during a further encryption operation in the second data processing means 17; the
30 encrypted data DA, can then be applied, via the second BUS connection 16, to the first data processing means 11 in which the encrypted data DA is further processed, after which, finally, load modulation is performed, via the connection 13B, in conformity with the encrypted data DA, thus yielding the load modulated carrier signal CSB in the receiver/transmitter means 4.

The sequencing means 15 provide control of the second data processing means 17 during the execution of such encryption operations, that is to say essentially in such a manner that the sequencing means 15 successively read the program instructions CO1, CO2 etc., via the fourth BUS connection 21, from the program P stored in the program storage means 20, after which a processing step, corresponding to the respective read program instruction, is executed in the second data processing means 17. During such processing of data DA by means of the second data processing means 17, under the control of the sequencing means 15 in conformity with the program P stored in the program storage means 20, a current peak pattern occurs at the area of the configuration of conductors 3 due to the data processing. The pattern configuration of the current peak pattern is then dependent on the program instructions CO1, CO2 ... COR, on the processed data DA, and on the characteristic value CV.

The data carrier 1, or the circuit 2, is preferably constructed in such a manner that the circuit 2 includes additional order fixation means 29 which co-operate with the sequencing means 15 and whereby, upon each execution of the algorithm formed by the program stored in the program storage means 20, an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms, so the N program blocks PB1, PB2 ... PBN.

In the present embodiment the order fixation means 29 include a random number generator 30. The random number generator 30 includes a supply input 31 via which the supply voltage V can be applied to the random number generator 30. The random number generator 30 is connected to the sequencing means 15, via a sixth BUS connection 32. Each random number Z generated by the random number generator 30 can thus be applied to the sequencing means 15 via the sixth BUS connection 32. The order fixation means 29, including the random number generator 30, are capable of fixing, upon each execution of the program P stored in the program storage means 20, an order which is determined by the random number Z generated by the random number generator 30 and is used for the execution of the N program blocks PB1 to PBN of the program P.

To this end, the order fixation means 29 additionally include order selection means 33 which are included in the sequencing means 15. The order selection means 33 contain feasible orders for the execution of the N program blocks PB1 to PBN of the program P. Preferably, the order selection means 33 contain only a part of all feasible orders. The order selection means 33 co-operate with the random number generator 30, that is to say in such a manner that the order selection means 33 can select an order from the feasible orders,

The first data processing means 11, the sequencing means 15, the second data processing means 17, the program storage means 20, the storage means 23 and the random number generator 30 constitute a respective circuit section of the circuit 2, which circuit sections can be supplied with the supply voltage V via the configuration of conductors 3.

The operation of the data carrier 1 and the circuit 2, respectively, in respect of the processing of data DA by means of the second data processing means 17 and under the control of the sequencing means 15 in conformity with the program P will be described in detail hereinafter with reference to the program blocks PB1 to PBN in Fig. 2.

When the second data processing cycle RUN2 is to be executed during the data processing operation, first the random number generator 30 is activated again, with the result that the random number generator 30 outputs a second random number Z2. The second random number Z2 is applied, via the sixth BUS connection 32, to the order selection means 33 so that the order selection means select a further order, for example the order PB6, PB3, PB7, PBN, PB1, ... PB4 and PB2 shown in the second column of Fig. 2. Thus, the second data processing cycle RUN2 involves a completely different order for the execution of the N

When the second data processing cycle RUN2 is to be executed during the data processing operation, first the random number generator 30 is activated again, with the result that the random number generator 30 outputs a second random number Z2. The second random number Z2 is applied, via the sixth BUS connection 32, to the order selection means 33 so that the order selection means select a further order, for example the order PB6, PB3, PB7, PBN, PB1, ... PB4 and PB2 shown in the second column of Fig. 2. Thus, the second data processing cycle RUN2 involves a completely different order for the execution of the N

program blocks. The order of the program instructions CO1, CO2 to COR etc., however, remains the same.

When the third data processing cycle RUN3 is to be executed in the course of the assumed data processing operation, the random number generator 30 is activated again in the same way as described above, so that the generator generates the random number Z3 and applies it, via the sixth BUS connection 32, to the sequencing means 15 or the order selection means 33 included therein. Consequently, the order selection means 33 select a further order for the execution of the N program blocks PB1 to PBN, for example the order PBN, PB1, PB4, PB6, PB3, ... PB7 and PB2 shown in the third column of Fig. 2. The third data processing cycle RUN3 thus involves a new order again for the execution of the N program blocks PB1 to PBN of the program P, the order of the program instructions CO1, CO2 to COR etc., however, again being the same.

As will be evident from the foregoing description, for the data carrier 1 shown in Fig. 1, or for the circuit 2 of the data carrier 1, it is achieved that, even though the order of all program instructions COX of all successively executed program blocks PBX is always the same upon each execution of the program P, the order for the execution of the N program blocks PBX of the program P is different during each execution of this program. It is thus achieved that the order of the execution of the N program blocks PBX cannot be detected from outside the data carrier 1 or the circuit 2 of the data carrier 1. Consequently, it is also impossible to compare successive orders of current peak patterns, caused by successive activation of the program P, in order to use such orders for analysis utilizing correlation methods, or to use the order of occurrence of the N current peak patterns, one of which occurs upon each execution of a program block PBX, for comparison methods. It is thus achieved that undesirable detection or recognition of the characteristic value CV used in the second data processing means 17 is practically impossible.

A further embodiment of data carrier (not shown) is provided with a wired logic circuit instead of the program storage means 20; this wired logic circuit co-operates with the sequencing means 15 and contains a wired algorithm, i.e. a hardware algorithm. This algorithm, stored hardware-wise in the wired logic circuit, enables analogous control of the second data processing means 17 by means of the sequencing means 15.

The invention is not restricted to the data processing device, so the data carrier 1, in the embodiment shown in and described with reference to Fig. 1. In the data carrier 1 shown in Fig. 1 the order selection means 33 are constructed so as to form part of the sequencing means 15, the order selection means 33 being realized in hardware. In a further

10

CLAIMS:

1. A data processing device (1) which includes a circuit (2) which consists of various circuit sections (11, 15, 17, 20, 23, 30) which can be fed with a supply voltage (V) via a configuration of conductors (3), and includes data processing means (17) which constitute such a circuit section that can be fed with the supply voltage (V) and are arranged to process data (DA) while utilizing a characteristic value (CV), and also includes sequencing means (15) which also constitute such a circuit section that can be fed with the supply voltage (V) and are arranged to execute an algorithm (P) in order to control the data processing means (17) in conformity with this algorithm (P), which algorithm comprises a given number N of sub-algorithms (PB1, PB2, ... PBN) which contain identical sequences of algorithm steps (CO1, CO2, ... COR) and can be executed in a given order each time when the algorithm (P) is executed, and wherein, upon processing of data (DA) by means of the data processing means (17) under the control of the sequencing means (15) in conformity with the algorithm (P), the data processing causes a current peak pattern to occur at the area of the configuration of conductors (3), the pattern configuration of the current peak pattern being dependent on the algorithm steps (CO1, CO2, ... COR), on the processed data (DA) and on the characteristic value (CV), characterized in that the circuit (2) additionally includes order fixation means (29) which cooperate with the sequencing means (15) and whereby, upon each execution of the algorithm (P), an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms (PB1, PB2, ... PBN).
2. A data processing device (1) as claimed in Claim 1, characterized in that the order fixation means (29) include a random number generator (30), and that, by means of the order fixation means (29) upon each execution of the algorithm (P), an order for the execution of the N sub-algorithms (PB1, PB2, ... PBN) is fixed, said order being defined by a random number (Z1, Z2, Z3) generated by the random number generator (30)
3. A data processing device (1) as claimed in Claim 2, characterized in that

the order fixation means (29) additionally include order selection means (33) which contain feasible orders for the execution of the N sub-algorithms (PB1, PB2, ... PBN) and co-operate with the random number generator (30), and

that the order selection means (33) can select an order from the feasible orders in conformity with a random number (Z1, Z2, Z3) received from the random number generator (30).

4. A data processing device (1) as claimed in Claim 1, characterized in that there are provided storage means (20) which co-operate with the sequencing means (15) and in which the algorithm (P) is stored in the form of a program which contains N program blocks as sub-algorithms (PB1, PB2, ... PBN) containing program instructions as algorithm steps (CO1, CO2, ... COR).

5. A data processing device (1) as claimed in Claim 1, characterized in that there is provided a wired logic circuit which co-operates with the sequencing means and contains the algorithm in wired and hence hardware form.

6. A data processing device (1) as claimed in Claim 1, characterized in that the data processing means (17) are formed by means for the encryption and/or decryption of data.

7. A data processing device (1) as claimed in Claim 1, characterized in that the data processing device (1) is formed by a data carrier whose circuit (2) is constructed in integrated technology.

8. A circuit (2) for a data processing device (1) which circuit consists of various circuit sections (11, 15, 17, 20, 23, 30) which can be fed with a supply voltage (V) via a configuration of conductors (3), and which circuit includes data processing means (17) which constitute such a circuit section that can be fed with the supply voltage (V) and are arranged to process data (DA) while utilizing a characteristic value (CV), and also includes sequencing means (15) which also constitute such a circuit section that can be fed with the supply voltage (V) and are arranged to execute an algorithm (P) in order to control the data processing means (17) in conformity with this algorithm (P), which algorithm comprises a given number N of sub-algorithms (PB1, PB2, ... PBN) which contain identical sequences of

algorithm steps (CO1, CO2, ... COR) and can be executed in a given order each time when the algorithm (P) is executed, and wherein,

upon processing of data (DA) by means of the data processing means (17) under the control of the sequencing means (15) in conformity with the algorithm (P), the data processing causes a

5 current peak pattern to occur at the area of the configuration of conductors (3), the pattern configuration of the current peak pattern being dependent on the algorithm steps (CO1, CO2, ... COR), on the processed data (DA) and on the characteristic value (CV), characterized in that

10 the circuit (2) additionally includes order fixation means (29) which co-operate with the sequencing means (15) and whereby, upon each execution of the algorithm (P), an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms (PB1, PB2, ... PBN).

9. A circuit (2) as claimed in Claim 8, characterized in that

15 the order fixation means (29) include a random number generator (30), and that by means of the order fixation means (29) upon each execution of the algorithm (P), an order for the execution of the N sub-algorithms (PB1, PB2, ... PBN) random number (Z1, Z2, Z3) generated by the random number generator (30).

20 10. A circuit (2) as claimed in Claim 9, characterized in that

the order fixation means (29) additionally include order selection means (33) which contain feasible orders for the execution of the N sub-algorithms (PB1, PB2, ... PBN) and co-operate with the random number generator (30), and

25 that the order selection means (33) can select an order from the feasible orders in conformity with a random number (Z1, Z2, Z3) received from the random number generator (30).

11. A circuit (2) as claimed in Claim 8, characterized in that

30 there are provided storage means (20) which co-operate with the sequencing means (15) and in which the algorithm (P) is stored in the form of a program which contains N program blocks as sub-algorithms (PB1, PB2, ... PBN) containing instructions as algorithm steps (CO1, CO2, ... COR).

12. A circuit (2) as claimed in Claim 8, characterized in that

there is provided a wired logic circuit which co-operates with the sequencing means and contains the algorithm in wired and hence hardware form.

13. A circuit (2) as claimed in Claim 8, characterized in that

5 the data processing means (17) are formed by means for the encryption and/or decryption of data.

14. A circuit (2) as claimed in Claim 8, characterized in that

10 the circuit (2) is intended for a data processing device (1) which is formed by a data carrier, and that the circuit (2) is constructed in integrated technology.

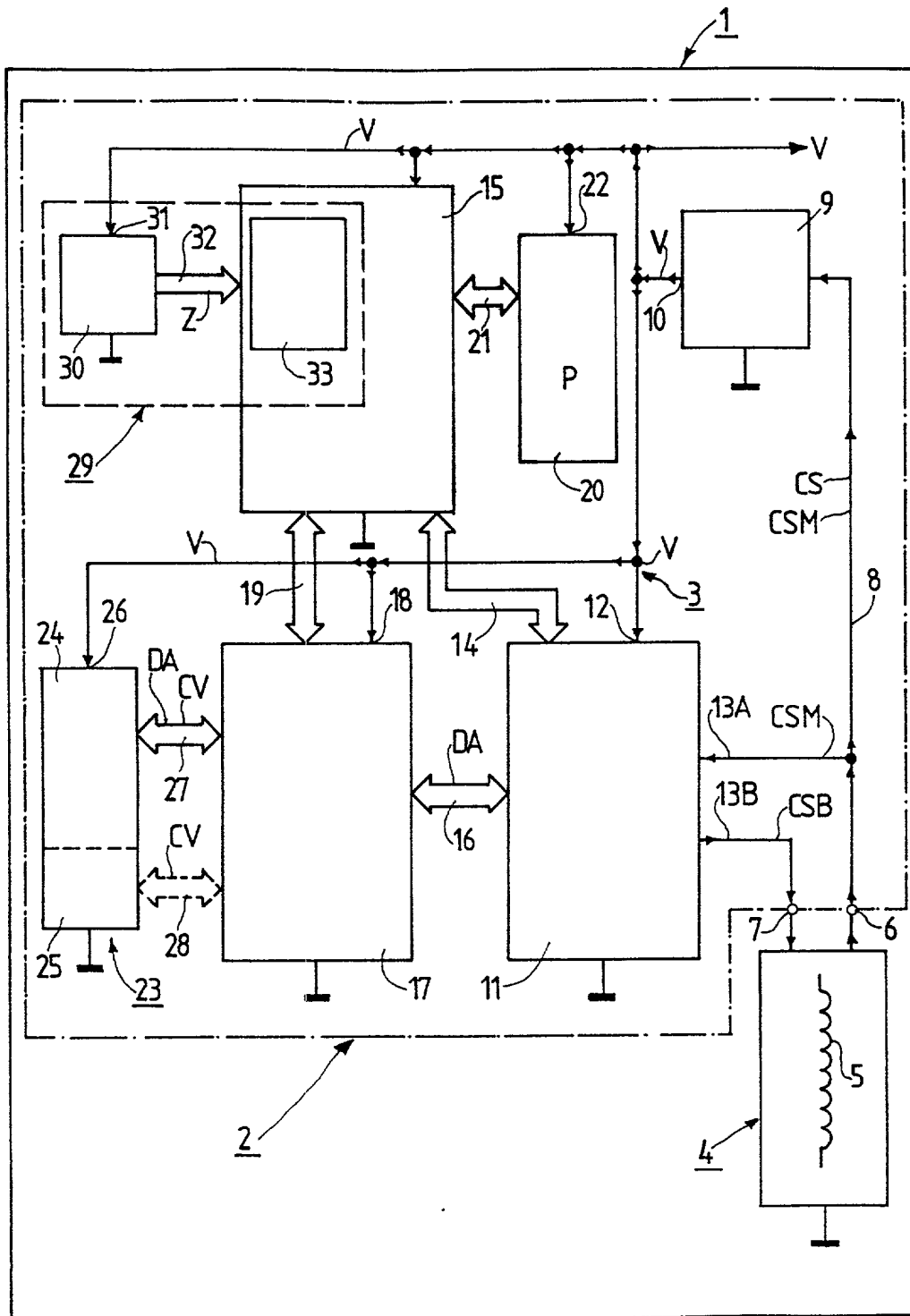
660620 443660

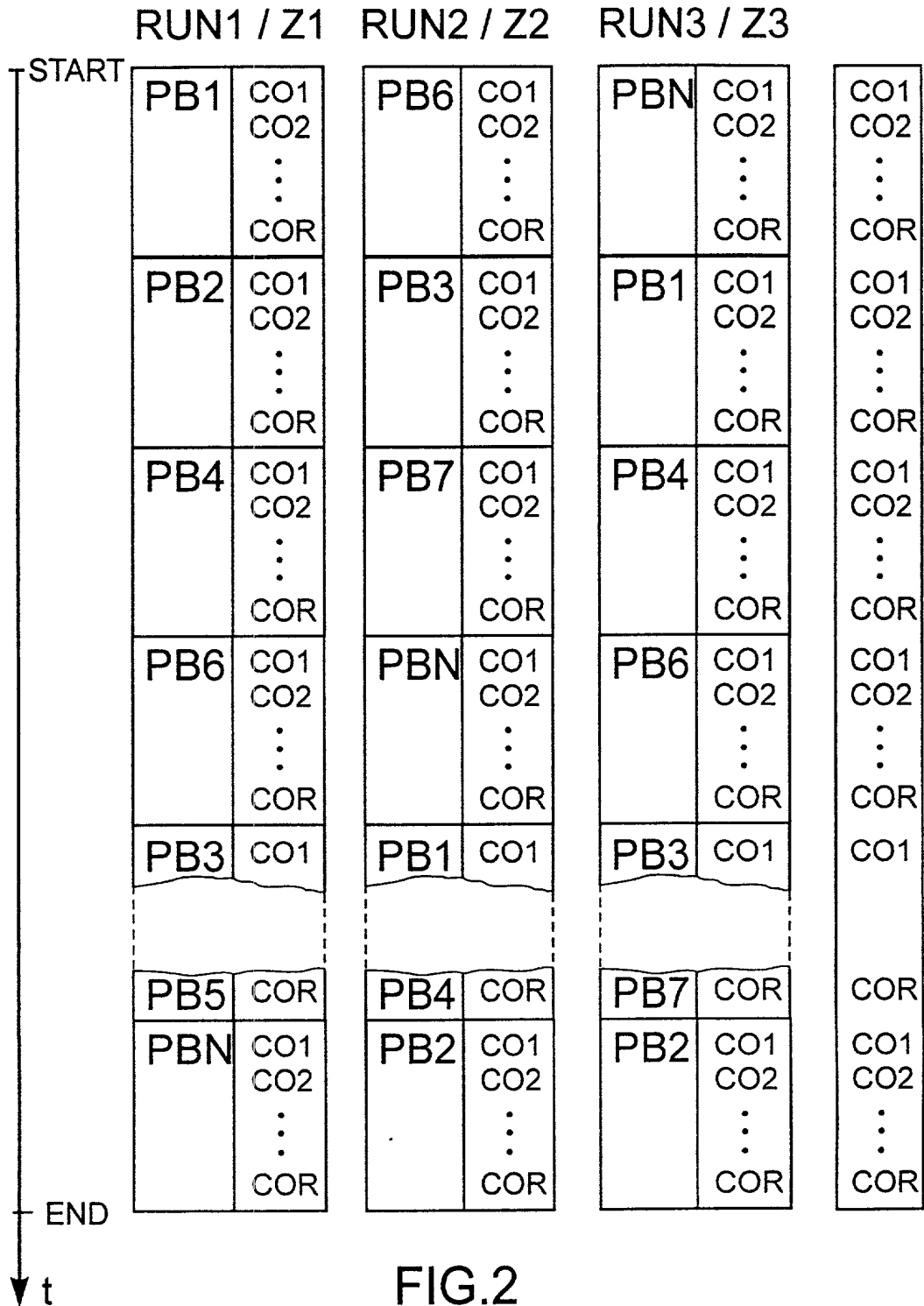
ABSTRACT:

A data processing device (1) which includes a circuit (2) with data processing means (17) which are suitable for processing data (DA) while utilizing a characteristic value (CV) and with sequencing means (15) which are arranged to execute an algorithm in order to control the data processing means (17) in conformity with this algorithm which comprises a
5 given number N of sub-algorithms containing identical successions of algorithm steps, is additionally provided with order fixation means (29) which co-operate with the sequencing means (15) and whereby, each time when the algorithm is executed, an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms.

10 (Fig. 1.)

660624 "F 23360





DECLARATION and POWER OF ATTORNEY

ATTORNEY'S DOCKET NO.:

PHO 98.532

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
"Data processing device with data processing means utilizing a characteristic value and with means for counteracting analysis methods for the detection of the characteristic value"

the specification of which (check one)

☐ is attached hereto.

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APP. NUMBER	DATE OF FILING (DATE, MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Europe	98890222.7	31 July 1998	YES

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Algy Tamoshunas, Reg. No. 27,677

Jack E. Haken, Reg. No. 26,902

SEND CORRESPONDENCE TO: Corporate Patent Counsel; U.S. Philips Corporation; 580 white Plains Road; Tarrytown, NY 10591	DIRECT TELEPHONE CALLS TO: (name and telephone No.) (914) 332-0222
--	--

Dated:		Inventor's Signature:	
Full Name of in Inventor	Last Name ULLY	First Name Klaus	Middle Name
Residence & Citizenship	City Deutschlandsberg	State of Foreign Country Austria	Country of Citizenship Austria
Post Office Address	Street Kirchengasse 7	City A - 8530 Deutschlandsberg	State of Country Austria
			Zip Code

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

KLAUS ULLY

PHO 98,532

Serial No.

Filed: CONCURRENTLY

Title: DATA PROCESSING DEVICE WITH DATA PROCESSING MEANS UTILIZING
A CHARACTERISTIC VALUE AND WITH MEANS FOR COUNTERACTING ANALYSIS
METHODS FOR THE DETECTION OF THE CHARACTERISTIC VALUE

Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all
prior appointments (if any) of Associate Attorney(s) or Agent(s) in
the above-captioned case and appoints:

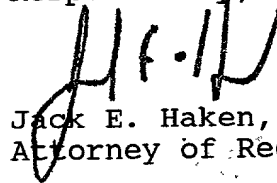
GREGORY L. THORNE

(Registration No. 39,398)

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580
White Plains Road, Tarrytown, New York 10591, his Associate
Attorney(s)/Agent(s) with all the usual powers to prosecute the
above-identified application and any division or continuation
thereof, to make alterations and amendments therein, and to
transact all business in the Patent and Trademark Office connected
therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE
LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED
ATTORNEY OF RECORD.

Respectfully,



Jack E. Haken, Reg. 26,902
Attorney of Record

Dated at Tarrytown, New York
this 27th day of July, 1999.